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09/510,974	02/21/2000	Rex Petersen	10001834	1706

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EXAMINER
WHITMORE, STACY

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>amendment filed 2/17/03</u> .

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-24</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-24</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>12 February 2000</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)   4)☐ Interview Summary (PTO-413) Paper No(s). _____ .

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)   5)☐ Notice of Informal Patent Application (PTO-152)

3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .   6)☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1.   Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ginetti et al. (6,170,080) in view of Jones et al. (5,629,860).

2.   As for claims 1 ,11 and claim 21, Ginetti taught the invention substantially as claimed, including A chip VLSI chip [col. 3, lines 25-32] who design was performed according to a method for VLSI chip design comprising the steps of:

(means for) estimating signal routes between functional blocks [col. 13, lines 53-56];

(means for) determining C values for the estimated signal routes [col. 14, lines 8-13]; and

(means for) building a model of said signal routes including C values [col. 14, lines] [the means for limitation is met by Ginetti's use of computer hardware and software]; and

wherein the design is in register transfer language [col. 3, lines 24-27].

Ginetti did not specifically disclose determining R values for the signal routes and building a model of said routes with R values.

Jones disclosed determining R values for the signal routes and building a model of said routes with R values [col. 7, line 30 –col. 8, line3; col. 10, line 65 col. 11, line 2].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ginetti and Jones because both Ginetti and Jones disclose methods of creating wiring load models for signal route delay purposes. Adding the R value to Ginetti's method would improve Ginetti's method by allowing for accurate delay estimates due to routing [see Jones, col. 7, line 30 – col. 8, line 3].

3.   As for claims 2 and 12, Ginetti taught foliating nodes in estimated signal routes [fig. 15, col. 10, lines 44-52: the netlist described reads on foliating nodes because the netlist is a list of connected points along estimated routes which have unique names such as those shown in figure 15. Applicant describes foliating nodes on page 8, lines 3-4, of the specification as giving unique names to each of the different points along an estimated route].

4.   As for claims 3 and 13, Ginetti taught generating a connectivity net list from said model [col. 3, lines 36-53].

5.   As for claims 4 and 14, Ginetti taught said step of estimating is performed based on input of a floor plan and a connectivity description [col. 1, lines 60-67: Ginetti discloses here that the netlist (connectivity description must be used with the floorplanner so capacitance and wire load models can be done, therefore estimating is done with the floorplanner and netlist].

6.   As for claims 5 and 15, Ginetti taught said step of estimating is performed in response to one or more control factor inputs [col. 13, lines 53-56; col. 12, lines 15-19; and col. 11; timing constraint files and design rule constraint file].

7.   As for claims 7 and 17, Ginetti taught said step of estimating is performed based on input of signal path configuration parameters [col. 13, lines 53-56; col. 12, lines 15-19; and col. 11; timing constraint files and design rule constraint file].

8.   As for claims 6, 8, 10, 16, 18 , and 20, Ginetti taught the invention substantially as claimed as cited in the rejection of claims 1, 4-5, 7, 9, 11, 14-15, and 17. Ginetti did not specifically disclose that said control factor input specifies a signal routing algorithm or that said signal route configuration parameters specify one or more signal path material, physical size of signal path material or spacing.

Jones disclosed a control factor input of a signal routing algorithm and signal route control parameters that specify one or more of signal path material, physical size of signal path material or spacing [col. 5, lines 17-48].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ginetti and Jones because Ginetti estimates signal routes between functional blocks including control factor inputs and signal route configuration parameters that would necessarily need an algorithm in order to perform routing as well as signal route characteristics in order to estimate the routing between blocks. Therefore, adding Jones disclosure of the use of specific control factor inputs such as signal routing algorithms (such as Steiner Tree method) and signal route configuration parameters (such as metal characteristics) would be useful for Ginetti's routing estimator.

9.   As for claims 9 and 19, Ginetti taught step of estimating is performed in response to one or more control factor inputs [col. 13, lines 53-56; col. 12, lines 15-19; and col. 11; timing constraint files and design rule constraint file].

10.   As for claims 22-24, Ginetti taught wherein the estimating signal routes between functional blocks occurs prior to a layout for the VLSI chip design [abstract; col. 1,].

11.   Applicant's arguments with respect to claims 1-24, have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy A Whitmore

Patent Examiner

Art Unit 2812

SAW

May 15, 2003